Patent Claims

1. A circuit arrangement for generating clock pulses in a communication system, the circuit arrangement (40) hasing at least one network termination (12 to 14), where each network termination (12 to 14) can be connected to at least one transmission line in each case and to a bus (18) and where a clock is provided for synchronizing the bus (18), characterized in that a multiplicity of clock generators (58, 41 to 44, 46) for generating the clock and means (47, 49) for selecting a clock generator (58, 41 to 44, 46) are provided.

2. The circuit arrangement as claimed in claim 1, characterized in that the means (47, 49) for selecting a clock generator (58, 41 to 44, 46) are programmable.

3. The circuit arrangement as claimed in claim 2, characterized in that the means (47, 49) for selecting a clock generator (58, 41 to 44, 46) are programmable via a register.

4. The circuit arrangement as claimed in one of claims 1 to 3, characterized in that the means (47, 49) for selecting a clock generator (58, 41 to 44, 45) has a first multiplexer (47), to whose inputs transmission lines can be connected and where the received signal of one of the transmission lines is used as clock generator.

5. The circuit arrangement as claimed in claim 4, characterized in that the circuit arrangement in each case have a phase control unit (PCU) preceding each input of the multiplexer, which derives a clock from the received signal of the

corresponding transmission line.

6. The circuit arrangement as claimed in claim 4 or 5, characterized in that the means (47, 49) for selecting a clock generator (58, 41 to 44, 46) has a second multiplexer (49), at the inputs of which the output signal of a phase locked loop (48) and a reference clock Refclk (46) are present.

7. The circuit arrangement as claimed in claim 6, characterized in that the phase locked loop (48) is supplied with a further clock from a crystal oscillator circuit (55 to 58) and the output signal of the first multiplexer (47) as input signals.

8. The circuit arrangement as claimed in one of claims 6 or 7, characterized in that three clock generators are provided, where a signal received via one of the transmission lines (41, 42, 43, 44) is used as first clock generator, the reference clock (46) is used as second clock generator and the combination of received signals from at least two transmission lines (41, 42, 43, 44) is used as third clock generator, where the clock generated by the third clock generator is generated, in particular, by averaging the clock information determined from the signals of the transmission lines (41, 42, 43, 44) involved.

9. The circuit arrangement as claimed in one of the preceding claims, characterized in that signals which are transmitted via the transmission lines (41, 42, 43, 44) correspond to the U interface protocol of ISDN.

10. The circuit arrangement as claimed in one of

claims 1 to 8, characterized in that signals which are transmitted via the transmission lines (41, 42, 43, 44) correspond to an XDSL protocol.

11. The circuit arrangement as claimed in claim 10, characterized in that the XDSL protocol corresponds to an ADSL or SDSL or VDSL or HDSL protocol.

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